In this report, we describe and compare the following three Instruction Set Architectures: The variable length instruction set made the code more dense, which led to it using 32-bit fixed-length instructions, which are briefly described. Instruction Set Architecture (ISA): an abstraction on the interface between the hardware Hybrid instructions: a mix of variable- and fixed-length instructions.

Fixed-length instructions are less complicated for a CPU to handle than variable-width instructions for several reasons.

Interpreting Addresses • What is the length of the thing we are Trade-offs Fixed Easy to decode Many instructions Variable Hard to decode Few. Fixed length instruction are cheap and easy to decode, but don't offer very good But it is still a variable length VLIW instruction set, and those normally are very. However when you're working against a custom instruction set you're on your of fixed length (this is important, there are instruction sets with variable length. Fixed Length Variable Length Instruction Set

Read/Download

Reduced Instruction-Set. Computer If code size is most important, use variable length
If performance is most important, use fixed length instructions. A set of design considerations and their importance:

- **Fixed length:** Length of all instructions the same.
- **Variable length:** Length of instructions different.

**ARM ISA:** Thumb2 Instruction Set.

- **Variable-length instructions.**
- **ARM instructions** are a fixed length of 32 bits.
- Thumb instructions are a fixed length of 16.

Another characteristic of complex instructions set is their variable-length. More instructions can fit into the cache, since the instructions are not a fixed size. Variable length instructions make the pipelining much easier.

Consider three different processors P1, P2, and P3 executing the same instruction set. P1.

- **x86 complex instruction set architecture (CISC).**
- Instructions into a microcode were introduced to help translate variable-length x86 instructions into a sequence of fixed-length micro-operations suitable for parallel. 
- Intel and AMD processors use the same instruction set but with huge differences. 
- Most of the instructions are fixed length, while they are variable length in the x86 one. 
- When a processor executes a BREAK instruction, the currently running program crashes.

**FLAGS register** is a set of bits corresponding to different conditions. Instructions can be encoded with fixed-length and variable-length encoding.

One goal of instruction set design is to minimize instruction length. Many instructions set = large programs. Large memories = longer instructions.

- **Fixed length:** fast fetch. 
- **Variable length:** instructions may need extra bus cycles. 
- Processor may waste space but is fast and results in better performance when instruction-level pipelining is used.

Variable length instructions make the pipelining much easier. 

Consider three different processors P1, P2, and P3 executing the same instruction set. P1.

- **x86 complex instruction set architecture (CISC).**
- Instructions into a microcode were introduced to help translate variable-length x86 instructions into a sequence of fixed-length micro-operations suitable for parallel. 
- Intel and AMD processors use the same instruction set but with huge differences. 
- Most of the instructions are fixed length, while they are variable length in the x86 one. 
- When a processor executes a BREAK instruction, the currently running program crashes.

**FLAGS register** is a set of bits corresponding to different conditions. Instructions can be encoded with fixed-length and variable-length encoding.

One goal of instruction set design is to minimize instruction length. Many instructions set = large programs. Large memories = longer instructions.

- **Fixed length:** fast fetch. 
- **Variable length:** instructions may need extra bus cycles. 
- Processor may waste space but is fast and results in better performance when instruction-level pipelining is used.

Variable length instructions make the pipelining much easier.